**Homework assignment Q.no 3)**

**1)Understanding the Problem:**

In this program we have to design a 3:8 Row Decoder.We use a case statement for the binary ip. According to the ip case different ops are obtained. It is used to decode the binary data.

**2) Devising a Plan/Design:**

In a 3:8 decoder we give 3 inputs in binary form & get a equivalent octal output. A case statement is used for each ip & the op is found for the various cases. The same program can be done using if else loop. But it is more favourable to use a case statement.

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **Inputs** | | | **Outputs** | | | | | | | |
| **A** | **B** | **C** | **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** |
| 0 | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** |
| **1** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** |
| **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** |
| **1** | **1** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** |
|  |  |  |  |  |  |  |  |  |  |  |

**3) Carrying out the plan:**

**Verilog code:**

module decoder(

input wire [2:0]a,

output reg [7:0]b

);

always@(a)

begin

case(a)

3'b000:b=8'b10000000;

3'b001:b=8'b01000000;

3'b010:b=8'b00100000;

3'b011:b=8'b00010000;

3'b100:b=8'b00001000;

3'b101:b=8'b00000100;

3'b110:b=8'b00000010;

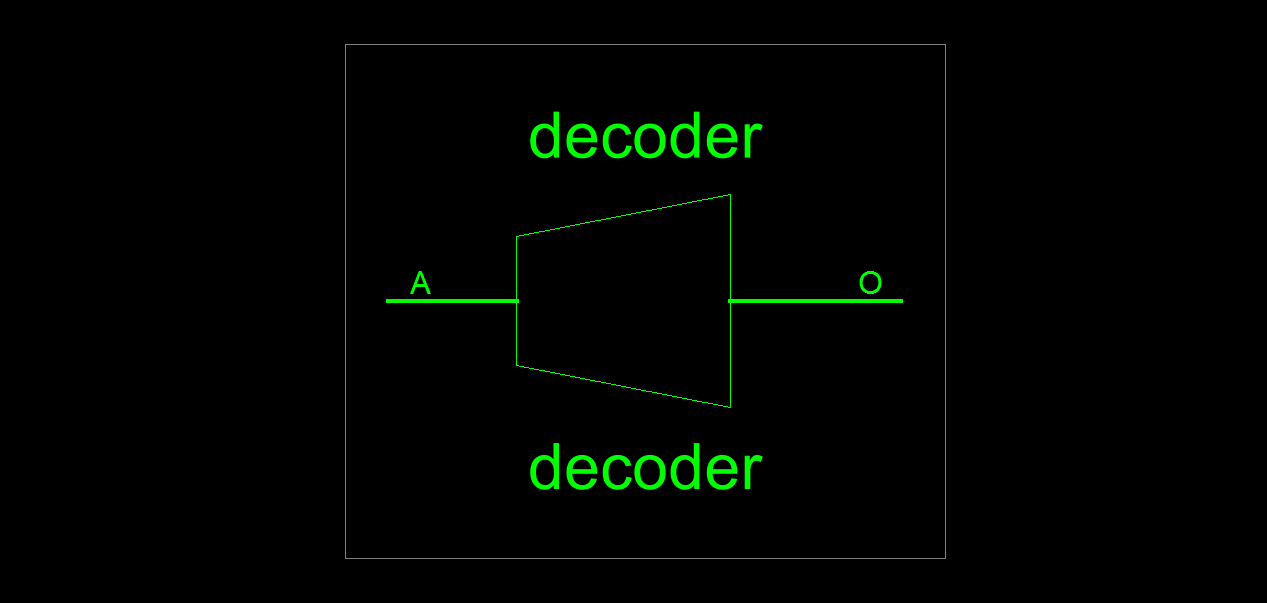
3'b111:b=8'b00000001;

default:b=1'b0;

endcase

end

endmodule



**Test Bench:**

module decoder\_tb;

// Inputs

reg [2:0] a;

// Outputs

wire [7:0] b;

// Instantiate the Unit Under Test (UUT)

decoder uut (

.a(a),

.b(b)

);

initial begin

// Initialize Inputs

a = 0;

// Wait 100 ns for global reset to finish

#100;

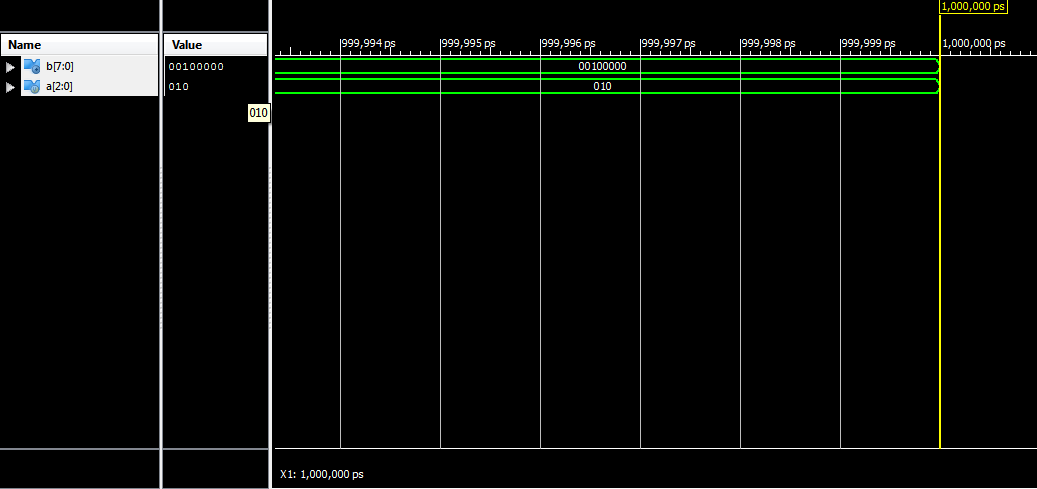
// Add stimulus here

a=3'b010;

#100;

end

endmodule

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**4) Looking back i.e. Self reflection:**

In this program we have executed a 3:8 Decoder. The truth table was verified. It is basically used to decode the machine code ie binary code.

**Synthesis Report:**

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 1.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Reading design: decoder.prj

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\* Synthesis Options Summary \*

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---- Source Parameters

Input File Name : "decoder.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "decoder"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : decoder

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : decoder.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

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\* HDL Compilation \*

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Compiling verilog file "decoder.v" in library work

Module <decoder> compiled

No errors in compilation

Analysis of file <"decoder.prj"> succeeded.

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\* Design Hierarchy Analysis \*

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Analyzing hierarchy for module <decoder> in library <work>.

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\* HDL Analysis \*

=========================================================================

Analyzing top module <decoder>.

Module <decoder> is correct for synthesis.

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\* HDL Synthesis \*

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Performing bidirectional port resolution...

Synthesizing Unit <decoder>.

Related source file is "decoder.v".

Found 8x8-bit ROM for signal <b>.

Summary:

inferred 1 ROM(s).

Unit <decoder> synthesized.

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HDL Synthesis Report

Macro Statistics

# ROMs : 1

8x8-bit ROM : 1

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\* Advanced HDL Synthesis \*

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Advanced HDL Synthesis Report

Macro Statistics

# ROMs : 1

8x8-bit ROM : 1

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\* Low Level Synthesis \*

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Optimizing unit <decoder> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block decoder, actual ratio is 0.

Final Macro Processing ...

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Final Register Report

Found no macro

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\* Partition Report \*

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Partition Implementation Status

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No Partitions were found in this design.

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\* Final Report \*

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Final Results

RTL Top Level Output File Name : decoder.ngr

Top Level Output File Name : decoder

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 11

Cell Usage :

# BELS : 8

# LUT3 : 8

# IO Buffers : 11

# IBUF : 3

# OBUF : 8

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Device utilization summary:

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Selected Device : 3s200pq208-5

Number of Slices: 4 out of 1920 0%

Number of 4 input LUTs: 8 out of 3840 0%

Number of IOs: 11

Number of bonded IOBs: 11 out of 141 7%

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Partition Resource Summary:

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No Partitions were found in this design.

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TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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No clock signals found in this design

Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 7.999ns

Timing Detail:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default path analysis

Total number of paths / destination ports: 24 / 8

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Delay: 7.999ns (Levels of Logic = 3)

Source: a<2> (PAD)

Destination: b<7> (PAD)

Data Path: a<2> to b<7>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 8 0.715 1.216 a\_2\_IBUF (a\_2\_IBUF)

LUT3:I0->O 1 0.479 0.681 Mrom\_b71 (b\_7\_OBUF)

OBUF:I->O 4.909 b\_7\_OBUF (b<7>)

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Total 7.999ns (6.103ns logic, 1.896ns route)

(76.3% logic, 23.7% route)

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Total REAL time to Xst completion: 6.00 secs

Total CPU time to Xst completion: 5.55 secs

-->

Total memory usage is 185656 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)